WE CLAIM:

1. Apparatus for processing data, said apparatus comprising:

a plurality of processor cores operable to perform respective data processing operations, at least two of said processor cores being operable in a coherent multi-processing mode sharing access to a coherent memory region; and

a memory access control unit coupled to said plurality of processor cores and operable to perform coherency management operations with respect to at least one cached copy of a data value from within said coherent memory region; wherein

at least one of said processor cores operable in said coherent multi-processing mode is coupled to a cache memory, said cache memory being operable to remain active to service coherency management operations issued by said memory access control unit whilst said processor core coupled to said cache memory is in an inactive power saving state.

2. Apparatus as claimed in claim 1, wherein said processor core coupled to said cache memory is not clocked in said inactive power saving state.

3. Apparatus as claimed in claim 1, wherein said cache memory is responsive to a copy coherency management request received from said memory access management unit to return a copy of a data value stored within said cache memory.

4. Apparatus as claimed in claim 1, wherein said cache memory is responsive to a status change coherency management request received from said memory access management unit to change a status value associated with a data value stored within said cache memory.

5. Apparatus as claimed in claim 1, wherein said cache memory is responsive to a clean coherency management request received from said memory access management

unit for a value stored within said cache memory to, if said value is dirty, then to return said dirty data value to a main memory.

6. Apparatus as claimed in claim 1, wherein in said inactive power saving state said processor core is responsive to a received interrupt signal to return to an active powered state.

7. Apparatus as claimed in claim 1, wherein a wait for interrupt instruction executed by said apparatus triggers said processor core to enter said inactive power saving state whilst said cache memory remains in said active state.

8. Apparatus as claimed in claim 1, wherein each of said processor core operable in said coherent multi-processing mode is coupled to a respective cache memory.

9. Apparatus as claimed in claim 1, wherein said apparatus comprises an integrated circuit including said plurality of processor cores, said memory access control unit and said cache memory.

10. A method of processing data, said method comprising the steps of:

performing data processing operations upon respective ones of a plurality of processor cores, at least two of said processor cores being operable in a coherent multi-processing mode sharing access to a coherent memory region; and

performing coherency management operations with respect to at least one cached copy of a data value from within said coherent memeory region using a memory access control unit coupled to said plurality of processor cores; wherein

at least one of said processor cores operable in said coherent multi-processing mode is coupled to a cache memory, said cache memory being operable to remain active to service coherency management operations issued by said memory access control unit whilst said processor core coupled to said cache memory is in an inactive power saving state.

11. A method as claimed in claim 10, wherein said processor core coupled to said cache memory is not clocked in said inactive power saving state.

12. A method as claimed in claim 10, wherein said cache memory is responsive to a copy coherency management request received from said memory access management unit to return a copy of a data value stored within said cache memory.

13. A method as claimed in claim 10, wherein said cache memory is responsive to a status change coherency management request received from said memory access management unit to change a status value associated with a data value stored within said cache memory.

14. A method as claimed in claim 10, wherein said cache memory is responsive to a clean coherency management request received from said memory access management unit for a value stored within said cache memory to, if said value is dirty, then to return said dirty data value to a main memory.

15. A method as claimed in claim 10, wherein in said inactive power saving state said processor core is responsive to a received interrupt signal to return to an active powered state.

16. A method as claimed in claim 10, wherein execution of a wait for interrupt triggers said processor core to enter said inactive power saving state while said cache memory remains in said active state.

17. A method as claimed in claim 10, wherein each of said processor core operable in said coherent multi-processing mode is coupled to a respective cache memory.

18. A method as claimed in claim 10, wherein said plurality of processor cores, said memory access control unit and said cache memory are part of a single integrated circuit.